Ultra High Temperature Emitter Pixel Development for Scene Projectors

Kevin Sparkman[a], Joe LaVeigne[a], Steve McHugh[a]

John Lannon[b] , Scott Goodwin[b]

[a]Santa Barbara Infrared, Inc., 30 S. Calle Cesar Chavez, #D, Santa Barbara, CA 93103

[b]RTI International, 3021 Cornwallis Rd., Research Triangle Park, NC 27709

ABSTRACT

To meet the needs of high fidelity infrared sensors, under the Ultra High Temperature (UHT) development program, Santa Barbara Infrared Inc. (SBIR) has developed new infrared emitter materials capable of achieving extremely high temperatures. The current state of the art arrays based on the MIRAGE-XL generation of scene projectors is capable of producing imagery with mid-wave infrared (MWIR) apparent temperatures up to 700K with response times of 5 ms. The Test Resource Management Center (TRMC) Test and Evaluation/Science & Technology (T&E/S&T) Program through the U.S. Army Program Executive Office for Simulation, Training and Instrumentations (PEO STRI) has contracted with SBIR and its partners to develop a new resistive array based on these new materials, using a high current Read-In Integrated Circuit (RIIC) capable of achieving higher temperatures as well as faster frame rates. The status of that development will be detailed within this paper, including performance data from prototype pixels.

Keywords: UHT, Scene Projection, LFRA, MIRAGE XL, WFRA, MIRAGE WF, MIRAGE II, Rise Time, Anneal, IRSP, pixel.

1. INTRODUCTION

Continuing their effort to extend the capability of resistive array based infrared scene projectors systems and support the United States Government's requirements for higher temperature projected scenes, Santa Barbara Infrared (SBIR) has fabricated resistive emitter pixels that reach higher apparent temperatures than are currently available in the commercial MIRAGE XL product line. The Ultra High Temperature (UHT)[1] Infrared Scene Projector (IRSP) program is developing new pixels that can reach the high apparent temperature needs of today's test applications. The technology used to produce the emitter array as well as the drive electronics were leveraged from the existing MIRAGE XL[2] and OASIS 1024[3] Infrared Scene Projection Systems. These new materials and pixels were developed with RTI International under the Ultra High Temperature program. This project is being funded by the Test Resource Management Center (TRMC) Test and Evaluation/Science & Technology (T&E/S&T) Program through the U.S. Army Program Executive Office for Simulation, Training and Instrumentations (PEO STRI). In addition to the new pixel materials and designs, a new Read in Integrated Circuit (RIIC) is also being developed to allow for scalable arrays up to 2Kx2k pixels.

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2. PROGRAM GOALS

The UHT program recently completed the first of its three program phases. In the first phase, new pixel designs were developed. The changes in mechanical design and layout were intended to mitigate localized stresses from material growth at high temperature. The program goals are to design a new RIIC and create a higher temperature pixel (Table 1). Several pixel designs were fabricated and tested as part of the first phase of the UHT program. New materials were also explored to achieve these higher temperatures. The material set used for LFRA,WFRA[4] and OASIS 1024 were not suitable for the extremely high physical temperatures dictated for the UHT program. SBIR and their collaborators explored new materials derived from lessons learned on the existing SBIR MIRAGE XL products. A suitable material set was found during the first phase of the program and use of those materials coupled with new pixel geometries led to over a 5 fold increase in radiance over the performance of existing legacy pixels.

In the second phase of the program, which just began in the spring of 2014, SBIR and their partners will continue the advancement of the pixel design and performance. SBIR will iterate on the increase in apparent temperature seen in the first phase pixels and enhance their performance for the maximum apparent temperature. In conjunction with the pixel enhancements, a new Read In Integrated Circuit (RIIC) will be developed. The existing RIICs available to the UHT program did not meet the demanding needs of the application. The RIIC for the UHT program needs the capability of being scaled from a relatively small 512x512 format to an ultimate goal of 2048x2048. This scalable RIIC does not currently exist. Traditional methods of designing a RIIC at a fixed size and the redesign to increase the size to the next step were not financially practical, nor were they technically achievable when yield was considered. To mitigate the lack of a suitable RIIC, a new scalable RIIC will be designed and fabricated in the second phase of the UHT program.

The third and final phase of the UHT program will deliver a complete turnkey system utilizing the new high temperature pixels. These pixels will be fabricated on the new scalable RIIC and packaged for use in a scene projector system. The system will include Command and Control Electronics (C&CE) for configuring the dynamic digital scene input for emitter array, and monitoring of all system functions. The power conditioning and thermal control will be provided by the Thermal Support System (TSS), which includes high current power supplies as well as the recirculating chiller to extract the heat generated by the resistive emitters. The emitter will be packaged inside an evacuated dewar capable of mounting on flight motion system as well as an optical bench.

Table 1. UHT system requirements and features

Parameter	Program Goal
Apparent Temperature Range (K) MWIR (3-5μm)	Cryo – 2000K
Spectral Range	3-14μm
Address Rate (full frame)	500Hz
Digital Resolution	14 bits
Operability (before NUC)	99.7%
Non-Uniformity (after NUC)	2%
Array Size	512x512
Spatial Resolution (pitch)	48 micron
Operating Temperature	50K to 300K

3. UHT RIIC

3.1 Legacy RIICS

The Ultra High Temperature program and delivery of the final system to a government test laboratory have definite needs. The Read in Integrated Circuit is the foundation of the projector on which most of the capabilities for system performance are derived. The RIIC defines the feature set for the format of the projected images. Whether it be the frame rate, aspect ratio or current per pixel, all of the parameters are dependent on the capability of the RIIC. The RIIC must be paired properly with the capabilities of the scene generation equipment and C&CE, as well as the pixel. The RIIC determines several factors, frame rate, array size, sub windows, and the drive current and voltage for each pixel. The RIIC also plays an important role in the spatial and temporal uniformity of the projected image. Deficiencies in the RIIC could have an adverse effect on the performance of the entire IRSP. For this reason, the UHT program will be embarking on the design of a new generation of RIICs suitable for the high temperatures and large formats required by today's test applications.

The RIIC used in the LFRA and WFRA designs as well as the OASIS 1024 program, while approaching the size needs of the UHT program, did not deliver enough current for each individual pixel. The emitter pixel currents required to achieve high temperatures for the UHT program were in excess of those available in the legacy RIIC designs of LFRA, WFRA and OASIS. Use of the 512x512 RIIC from Nova Sensors, A Teledyne Majority Owned Company was explored. The NOVA-15 RIIC, while having enough emitter pixel current capability, had a fixed format of 512x512 pixels. Additionally, uniformity concerns and the lack of testability and availability have led the UHT program to move away from this design in favor of a RIIC designed with quilting and scalability in mind.

3.2 UHT RIIC requirements

As mentioned in the section above, current RIICs cannot source enough current to drive a pixel to temperatures well over 1000K. In addition to the high temperature focus of the UHT program, there are other enhanced performance requirements that the system must support. These include operation at frame rates up to 500 Hz, operation at near room ambient and cryogenic temperatures and a path from the 512x512 demonstrator to arrays up to 2048x2048 or larger.

Current pixel models predict up to 10mW per pixel being required to achieve apparent temperatures over 1500K at with rise/fall times of 2ms. This amount of power per pixel is an order of magnitude higher than that which the legacy RIICs can support and will require a new unit cell design to support it. The large array support drives the design to a tiled architecture. This, in turn, leads to other requirements. One requirement is that that the RIIC support Through Silicon Vias (TSVs) for signal and emitter current

distribution across the chip. Bringing all the current required for a tile from a single side would lead to significant buss bar robbing effects. Tiling anything 3x3 or larger requires signals and biases to be brought in from the back of the RIIC as well. Moving to a tiled architecture places requirements on alignment between the tiles, which must be aligned to within much less than a pixel pitch. In order to limit artifacts at the seams, the tiles must have a gap considerably smaller than the pixel pitch. The alignment and gap requirements are both addressed through the use of Quilt Packaging (QP) to align and join the tiles together. Both TSVs and Quilt Packaging are discussed in more detail in the paper "Scalable emitter array development for infrared scene projector systems". See Table 2 for a list of RIIC requirements.

Table 2. Table of preliminary RIIC SPECS

Parameter	Prior* Performance	Ultimate Goal
Format	1024 x1024 fixed	4K x 4K (512x512 tiles quilted, variable)
TSV compatible	N/A	yes
Address Rate (full frame)	200Hz	1KHz
Manufacturability (RIIC yield)	10-15%	75 - 80%
Emitter voltage	5V	10V
Unit cell current	200uA	>1000uA
Digital Resolution	14 bits	16 bit
Operability (before NUC)	99.5%	99.9%
Uniformity (after NUC)	3%	<1%
Spatial Resolution (pitch)	48 micron	48 micron (Baseline)
Operating Temp	245K to 300K	80K to 300K

*Based on MIRAGE-XL system performance

4. UHT PIXELS

One of the primary goals of the UHT program is to develop pixels capable of achieving very high apparent temperatures. The current state of the art scene projector (OASIS and MIRAGE-XL) pixels achieve 650-700K MWIR apparent temperature. In both of the systems mentioned above, the limiting factor in the pixel apparent temperature is the physical temperature of the pixels themselves. The apparent temperature of an object is the temperature of an ideal blackbody radiator that would produce the same in-band. Real pixels have less than 100% fill factor and have less than unit emissivity. The radiance of a pixel at temp T_{pixel} on a substrate at temperature T_{sub} and in an ambient environment of temperature T_{amb} can be written as:

$$L_{pix} = L\ (T_{pix}) * \varepsilon_{pix} * ff + L\ (T_{amb}) * (1 - \varepsilon_{pix}) + L(T_{amb}) * (1 - \varepsilon_{sub}) + L\ (T_{sub}) * \varepsilon_{sub}$$

Where ε_{pix} is the in-band emissivity of the pixel, ε_{sub} is the in-band emissivity of the substrate and ff is the fill factor of the active area of the pixel. In the MWIR band, for temperatures much higher than ambient, the contributions from ambient reflections and substrate emissivity are negligible and the equation can be simplified to:

$$L_{pix} = L\ (T_{pix}) * \varepsilon_{pix} * ff$$

The apparent temperature of the pixel can then be written as:

$$L(T_{app}) = L\ (T_{pix}) * \varepsilon_{pix} * ff$$

The above does not have a closed form solution for T_{app} and so it is solved numerically.

Starting with the second equation, we can infer an approximate physical temperature of a pixel based on its apparent temperature. For the MIRAGE-XL system, pixels have a fill factor of 62.5% and the MWIR emissivity is estimated to be near 0.8. At apparent temperatures near 700K[5], the physical temperature of the pixel is over 800K. Figure 1 shows a scanning electron microscope (SEM) image of a MIRAGE-XL pixel.

Recently, many test pixels were produced under the UHT program as part of the path towards the goal of a high temperature pixel. These pixel structures were tested using a source meter (Keithley 2601) to simultaneously measure voltage and current going into the pixels as well as concurrent radiance measurements using an IR camera (IRCameras IRC800). Pixels were driven between zero and a set current with a period of approximately 1 second and a 50% duty cycle. The desired current was gradually increased and current, voltage and radiance measurements collected while the pixel was operating. Figure 2 shows a section of measurements from a typical pixel test run.

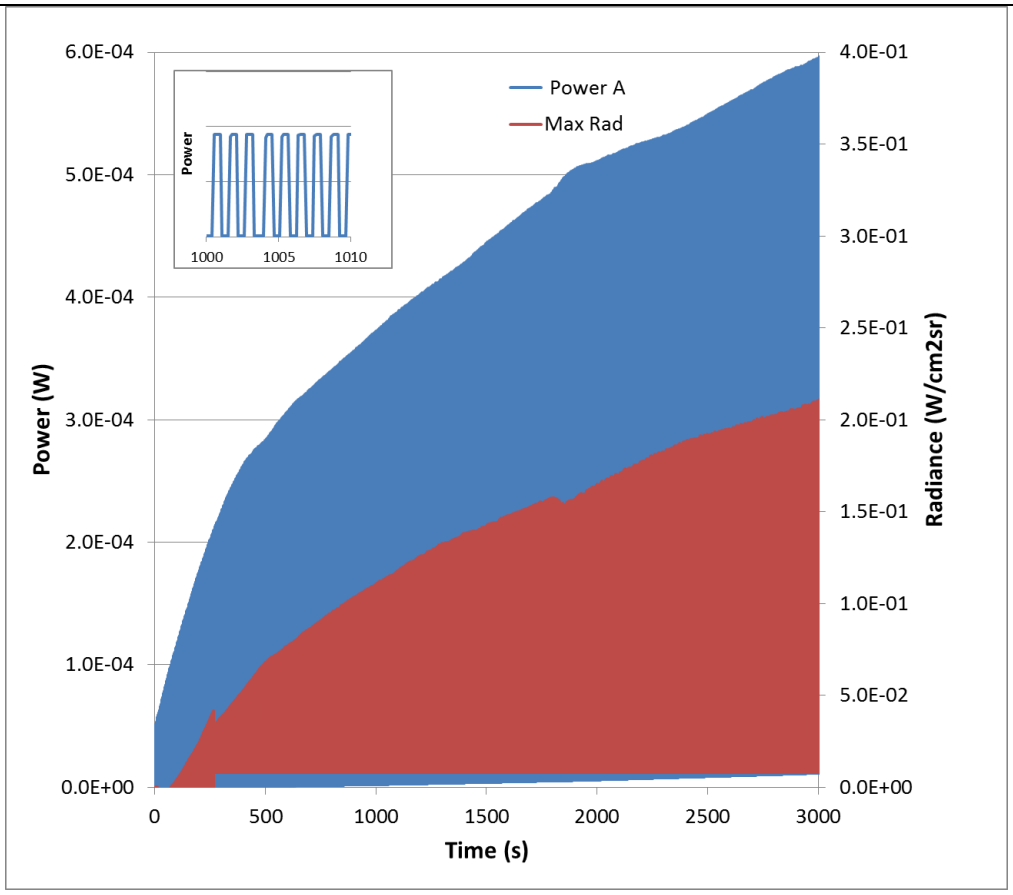

Figure 1 Portion of a typical pixel test.

The new pixel materials achieved a significantly higher MWIR radiance output than previous pixels. The maximum stable apparent temperature achieved using the test pixels was 1030K. Figure 3 shows a plot of MWIR radiance as a function of apparent temperature, annotated with the maximum temperature of various existing systems and the current UHT results. The UHT pixels have a similar emissivity to that of the legacy pixels, but have a fill factor of near 80%, considerably higher than legacy pixels. Figure 2 shows a SEM image of the UHT design that achieved an apparent temperature of over 1000K. Using the same technique as earlier, the maximum physical temperature is estimated to be over 1150K.

Although the pixels survived much higher physical temperatures and radiance output was increased over 5x that of legacy systems, the pixels in this test lot exhibited some unsatisfactory traits. The main issue was a 10x drop in resistance as the pixel was heated from ambient to >1000K. Although the source meter has the range to accommodate such a large temperature coefficient of resistance, no current or planned RIIC design supports one so large. Further investigation showed the resistance change was due to the dielectric pixel body becoming slightly conductive at high temperatures. Although the conductivity of the dielectric was much lower than that of the resistive element, the relative geometry of the elements led dielectric conductance to overwhelm that of the resistor. Another lot of test pixels is currently underway with a modified dielectric material. These pixels are expected to achieve MWIR apparent temperatures of up to 1500K with rise and fall times on the order of 2 ms.

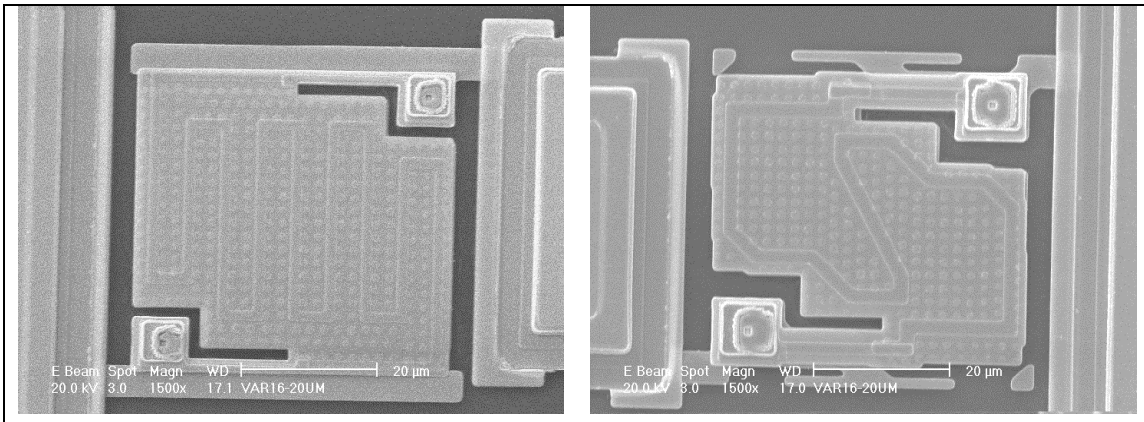

Figure 2. Comparison of UHT and MIRAGE-XL pixel format. Note the UHT pixel has a higher fill factor than the MIRAGE-XL pixel.

4.1 Expected Performance of final UHT pixel

The UHT program will increase the performance envelope for scene projection systems using resistive arrays. The UHT program will increase the maximum apparent temperature while improving the rise time of the pixels for resistor array IRSP systems. Relative performance can be seen in Figure 3.

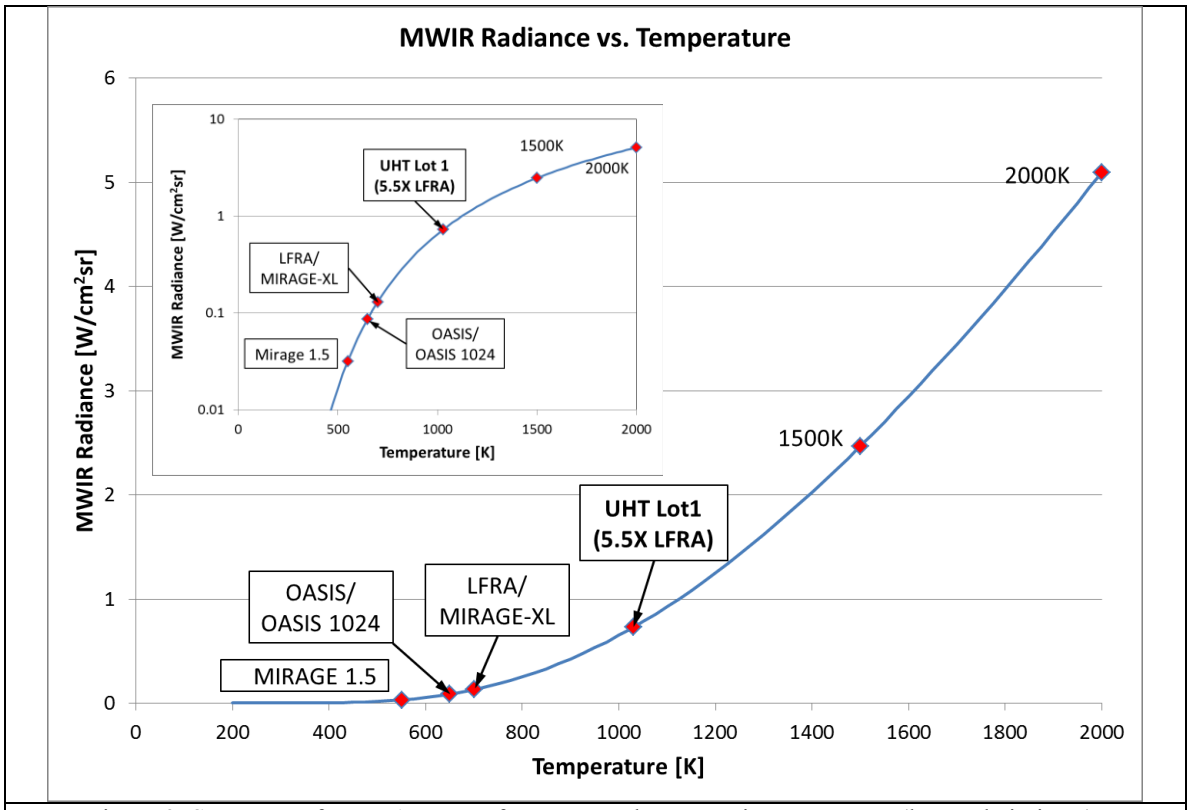

Figure 3. Summary of UHT Array Performance vs legacy emitter programs (log scale in inset).

5. SUMMARY

The Ultra High Temperature pixels have shown tremendous advancement in radiant output levels compared to legacy scene projector levels. This 5.5x increase in radiance is from a careful study and analysis of materials as well as fabrication of test pixels. From over twenty pixels variations of materials and physical configurations several have been selected to carry forward into the next phase of the program. The foundation of high temperature and radiance output pixels will be built upon in the coming phase to further increase the apparent temperature of the resistive emitter based infrared scene projectors. Paired with the advancement in performance of the pixels will be a new scalable Read in Integrated Circuit. This scalable RIIC will use quilt packaging and Through Silicon Vias to achieve extremely large arrays, up to 4Kx4K. The next generation RIIC will be based on 512x512 tiles to take advantage of the excellent yield in this configuration.

DISCLAIMER

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Any opinions, findings, and conclusions or recommendations expressed in this material are those of the author(s) and do not necessarily reflect the views of the Test Resource Management Center (TRMC) and Evaluation/Science & Technology (T&E/S&T) Program and/or the U.S. Army Program Executive Office for Simulation, Training, & Instrumentation (PEO STRI).

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