MIRAGE: Developments in IRSP System Development, RIIC Design, Emitter Fabrication, and Performance

Paul Bryant, Jim Oleson, Brian Lindberg, Bruce Anderson, Kevin Sparkman, Steve McHugh
Santa Barbara Infrared, Inc., 30 S. Calle Cesar Chavez, Suite D, Santa Barbara, CA 93103

John Lannon, David Vellenga, Scott Goodwin
MCNC-RDI, 3021 Cornwallis Rd., Research Triangle Park, NC 27709

Steve Solomon
Acumen Consulting, P.O. Box 6084, Santa Barbara, CA 93160

ABSTRACT

SBIR's family of MIRAGE infrared scene projection systems is undergoing significant growth and expansion. SBIR has completed the transition of Honeywell's resistive emitter technology to MCNC Research and Development Institute (MCNC-RDI), and is preparing for first-lot production of IR emitters in support of ongoing programs. Development of MIRAGE resistive emitter-based products is underway in order to increase maximum scene temperature, decrease radiance rise time, and improve overall operation. The 1024 x 1024 Large Format Resistive Array (LFRA) Read-In Integrated Circuit (RIIC) has been fabricated and tested, with emitter fabrication to start in mid-2003. A next-generation MIRAGE II (512 x 512) RIIC is also ready for fabrication, in support of high-performance MIRAGE II 512 x 512 systems providing greater than 750 K MWIR apparent temperature, and less than 5 ms 10-90% MWIR radiance rise time. In support of these new technologies and products, SBIR has developed test equipment and facilities for use in next-generation MIRAGE device wafer probing, test, evaluation, diagnostic, and assembly processes.

Keywords: Command & Control Electronics, Emitter Array, IR Scene Projection, MEMS Fabrication.

1. INTRODUCTION

Resistive emitter-based IRSP technology still leads the industry in terms of a flickerless, high dynamic range test solution. The last year has seen significant technical developments in the next-generation of SBIR's MIRAGE IR scene projection systems. The exclusive Honeywell emitter technology license signed in 2001 has been completed, and a transfer foundry (MCNC-RDI) has been brought on line. Fabrication of a prototype emitter lot has been completed at MCNC-RDI, and devices are currently in test. Large-format 1024 x 1024 RIICs have been designed, produced, and tested. The next-gen MIRAGE II (512 x 512) RIIC has completed design, and is ready for fabrication in 2003. The next-gen C&CE architecture has been defined, and the core technology is being tested and integrated in preparation for upcoming system deliveries. Significant calibration/radiometry system (CRS) upgrades are also underway, with new optics, a full-array/sparse-grid collection scheme, and software algorithms under development.

2. EMITTER FOUNDRY

Following a successful emitter fabrication run at Honeywell in 2002, the resistive emitter process has been transferred to the MCNC-RDI - a world-class organization with a strong background in MEMS design and fabrication. The technical team at MCNC-RDI has completed both phase 1 and phase 2 technical startup activities. Phase 1 consisted of material and process development for the crucial emitter films and layers comprising the basic pixel structure. Phase 2 involved production of one lot of "MIRAGE 1.5" arrays. The MIRAGE 1.5 configuration incorporates exclusively-licensed Honeywell Labs emitter technology onto MIRAGE 1 CMOS. The goal was to duplicate the device structural and performance features demonstrated by Honeywell and SBIR in 2002, and thus establish MCNC-RDI's readiness to move on to

production fab.

Phase 1 material/process development involved numerous test depositions and processing steps related to emitter metal films, dielectric stacks, leg metals, absorber films, reflector films, plug metals, and typical MEMS sacrificial layers. Phase 1 also proved-in the ability to duplicate the baseline pre-/post-anneal characteristics for the emitter metal – a key step toward producing emitter films with predictable, well-understood thermal and electrical characteristics. Also developed in phase 1 were the key processing steps related to patterning, etching, and ion milling – essential capabilities requiring a high degree of control and repeatability.

Fabrication of prototype emitters in phase two involved read-in integrated circuit (RIIC) wafer preparation, followed by a complete fabrication run using the baseline recipes developed in phase 1. Phase 2 fabrication also included two "lot splits" in which a few selected wafers were used for development of improved reflector metal and bridge dielectric materials. Devices from the experimental wafers will be used to validate specific performance and yield improvement techniques for possible use in future production runs. There were a great many technical challenges and lessons learned in phase 2, but the MCNC-RDI/SBIR team was able react successfully at all decision points, resulting in successful prototype devices. Figures 1a and 1b show both "standard" and "gossamer" pixel and array images. As the photos illustrate, film deposition and lithographic quality was high, and the arrays physically look as good or better than the devices produced at Honeywell in 2002 during the technology license validation run.

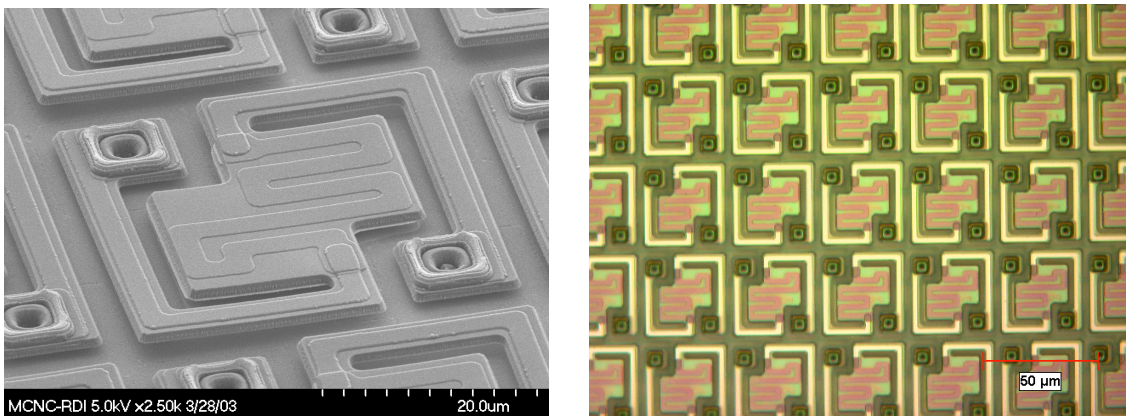

Figure 1a –MCNC-RDI/SBIR Standard Validation Pixel (left) & Array Close-Up (right)

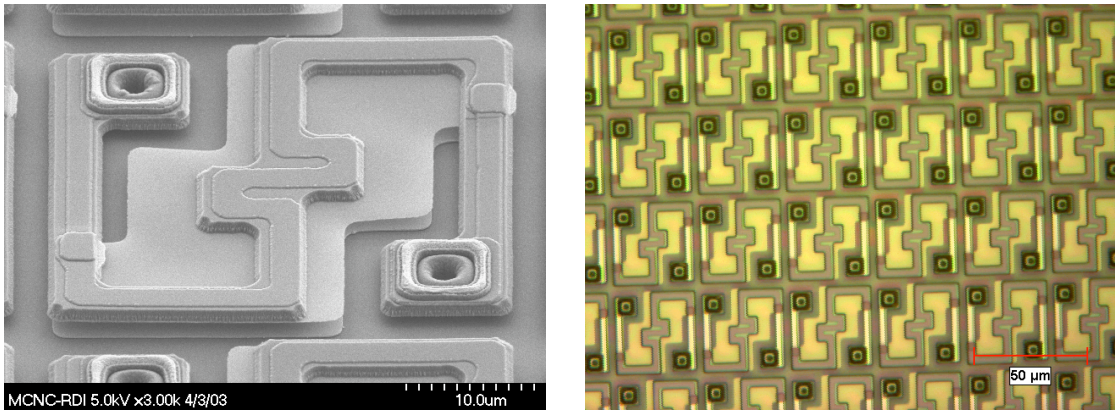

Figure 1b – MCNC-RDI/SBIR Gossamer Validation Pixel (left) & Array Close-Up (right)

The first MCNC-RDI MIRAGE 1.5 arrays are undergoing test at SBIR, and performance data will be available shortly. Array performance, operability, and anneal characteristics will be used to judge the success of the prototype fab run, and clear the way for the first production lots scheduled for later in 2003. Theoretical performance for MIRAGE 1.5 arrays is shown in table 1. Early indications of emitter resistance measured on test pixels at MCNC-RDI suggest that prototype performance will be quite close to these levels.

	STANDARD PIXEL	GOSSAMER PIXEL
MWIR Apparent Temperature	> 600 K	> 500 K
MWIR Radiance Rise Time	< 10 ms	< 5 ms
Frame Rate	20-200 Hz	
Array Configuration	512 x 512	
Unit Cell Size	39 x 39 □m	
Frame Update Modes	Snapshot, Raster	

Table 1 - MIRAGE 1.5 Performance Specifications

MIRAGE 1.5 arrays will be offered with both standard and gossamer pixel types to provide "in-production" solutions optimized for either maximum temperature or speed – prior to availability of the first MIRAGE II devices.

3. MIRAGE II (512 x 512) DEVELOPMENT

Using the last few years of MIRAGE development as a point of departure, SBIR is embarking on several aggressive new product development activities to advance the state-of-the-art in turn-key IRSP systems. UUT performance is evolving at a rapid pace, and simulation system performance must grow accordingly. Many hardware-in-the-loop (HWIL) test applications call for MWIR apparent temperatures of 700-800 K, with even more stressing future "hot spot" requirements – on the order of 2500 K! The thrust toward faster radiance rise and fall times continues, with current requirements less than 5 ms (10-90 % rise/fall), and goals of 2 ms on the horizon. In addition to performing research in the area of very high temperature materials and processes, SBIR is developing the core technologies and devices required to support current and emerging IRSP needs. As illustrated in figure 2, MIRAGE II and LFRA are extending the previous performance frontier, with significant headroom available for annealing and advanced emitter materials R&D.

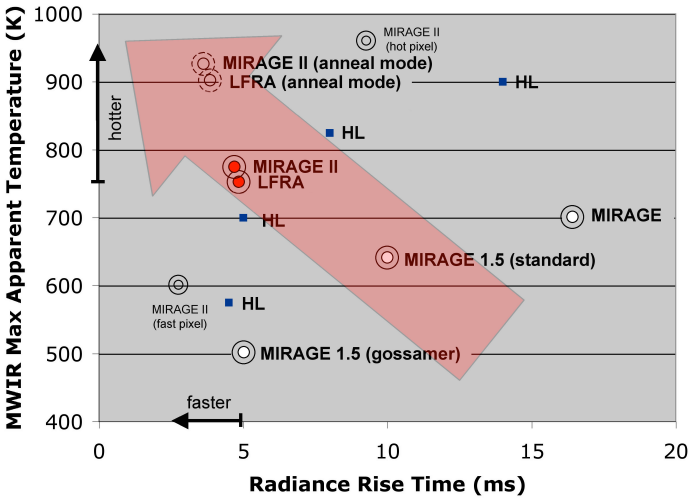

Figure 2 – IRSP Performance Trends

In order to extend the capabilities of the original MIRAGE system and take full advantage of the latest resistive emitter technology, an improved 512 x 512 scene projector array design is complete and ready for CMOS fabrication. The array incorporates four on-chip DACs (vs. two on MIRAGE), delivers up to 800 μW of power to each emitter in projection mode (vs. 200 μW on MIRAGE), runs at frame rates up to 400 Hz (vs. 200 on MIRAGE), provides a dedicated anneal mode, and includes extensive test capabilities. The MIRAGE II array floor plan is shown in figure 3b. The MIRAGE II RIIC will be fabricated using the same AMI Semiconductor process as the LFRA chip, and will exploit the advantages of "stitched" IC fabrication, whereby the silicon wafer is exposed in multiple steps to pattern each individual die and the complete wafer. Circuit layout is performed such that the glass mask includes a selection of circuit/layout blocks, which may be stepped, repeated, and combined to create the full wafer pattern. The approach is illustrated in figure 3a.

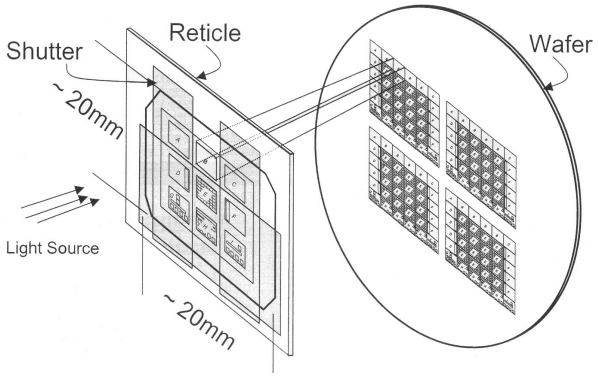

Figure 3a – "Stitched" Photolithographic Technique

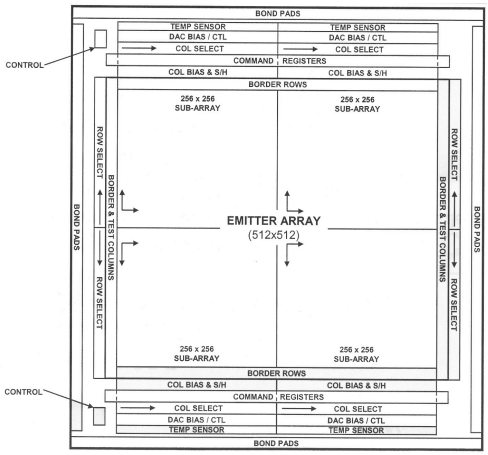

Figure 3b – MIRAGE II Array Floor Plan

The stitched technique allows fabrication of large devices, unrestricted by traditional limitations in mask reticle size, and allows CMOS designs to be created with inherent scalability to larger array configurations. The MIRAGE II RIIC offers very high pixel level performance, and with emitters fabricated at MCNC-RDI, will offer a dramatic improvement over performance demonstrated on MIRAGE 1. A comparison of MIRAGE II and MIRAGE 1 performance is shown in table 2.

	MIRAGE II	MIRAGE 1
Apparent Temperature (MWIR)	> 750 K	~ 700
Apparent Temperature (LWIR)	> 600 K	~ 500 K
Radiance Rise Time	< 5 ms	~ 17 ms
Frame Rate	20-200 Hz	
Array Configuration	512 x 512	
Unit Cell Size	48 x 48 μm	39 x 39 μm
Frame Update Modes	Snapshot, Raster	

Table 2 – Comparison of MIRAGE II and MIRAGE 1 Performance

4. LARGE-FORMAT (1024 x 1024) DEVLOPMENT

The key LFRA requirements provided by the Tri-Services IRSP working group, plus selected RIIC flow-down specs are summarized in Table 3. The LFRA is specified to produce apparent temperatures in excess of 700 K in the MWIR (3-5 μm), and greater than 500 K in the LWIR (8-12 μm). Radiance rise time (10-90%) is specified to be less than 5 ms, and the LFRA will support this with margin, particularly in the LWIR. The array must operate at frame rates between 20 Hz and 200 Hz in normal 1024 x 1024 mode (full-frame), and at frame rates up to 400 Hz in 512 x 1024 window mode.

LFRA PROJECTOR ARRAY REQUIREMENTS	
Apparent Temperature (max)	> 700 K (MWIR)
	> 500 K (LWIR)
Radiance Rise Time	< 5 ms (MWIR)
	< 4.5 ms (LWIR)
Frame Rate	20-200 Hz (full-frame)
	Up to 400 Hz (window-mode)
Array Configuration	1,024 x 1,024
Unit Cell Size	48 x 48 μm
Frame Update Modes	Snapshot, Raster
Windowing	512 x 1,024 - static

LFRA RIIC FLOW-DOWN REQUIREMENTS	
Emitter Drive Mode	Current
Emitter Resistance (nom)	20 kΩ
Emitter Drive Power	700 μW (spec)
	800 μW (goal)
Drive Resolution	> 14-bit effective
Anneal Mode Headroom	> 10 % (power)

Table 3 – LFRA Specifications & Flow-Down Requirements

The very large, 2 x 2-inch LFRA RIIC architecture is shown in Figure 1. The core is partitioned into eight 256 x 512 regions, each served by a dedicated digital-to-analog converter (DAC) stage. Figure 4a illustrates the RIIC floor plan. Fabrication has been completed at AMI Semiconductor, and wafer testing is in progress. A finished LFRA wafer containing five RIIC devices is shown in figure 4b.

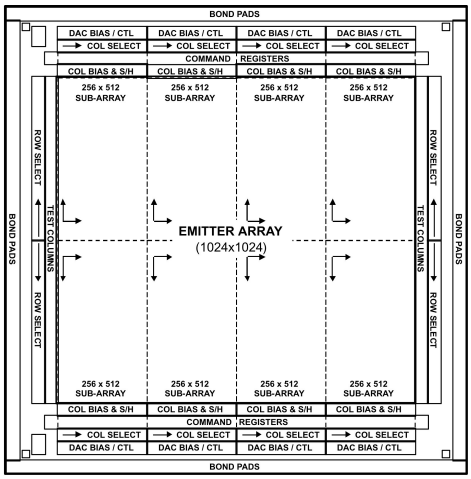

Figure 4a – LFRA RIIC Floorplan

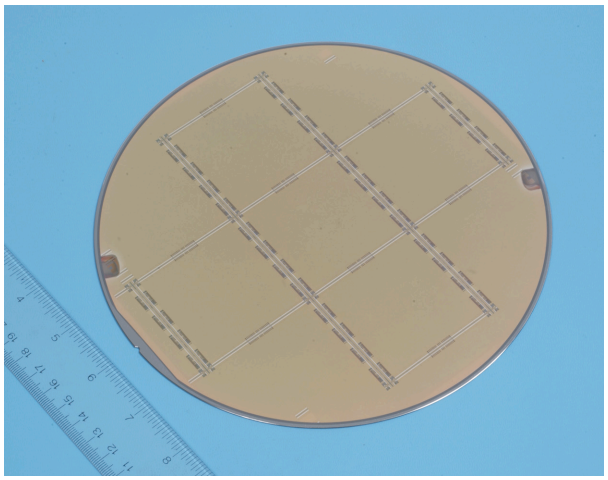

Figure 4b – LFRA (1024 x 1024) Wafer

The left and right sides of the array are populated with a large number of unit cell electrical power supply pads, in order to minimize power supply variation as a function of dynamic scene content. All other clock, bias, and digital input data functions reach the LFRA RIIC via the top and bottom edges of the chip.

5. NEXT-GENERATION C&CE

Development is proceeding on the next-generation MIRAGE C&CE, which will feature a brand-new architecture and support MIRAGE 1.5, II, 1024, and future configurations. The new MIRAGE C&CE is a standard PCI-based unit incorporating a single-board computer/host for control/GUI use, and a variety of input, processing, output, communications, and peripheral cards as shown in figure 5. The C&CE receives data from the scene generation platform, performs real-time non-uniformity correction (NUC) and data processing functions, and streams fiber-optic digital data and timing signals to the DEE.

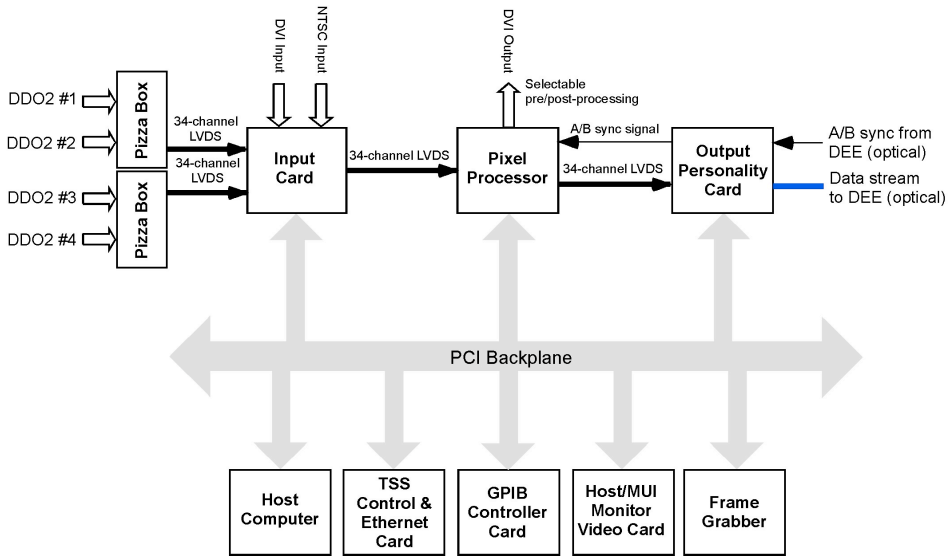

Figure 5 – Next-Gen C&CE Block Diagram

Scene data is transmitted in DDO2/DVP2 format via PECL-to-LVDS "pizza box" converters, or in DVI format directly to the Timing & Input Processor (TIP) card. The TIP also accepts NTSC input, serves as internal clock/sync master for the C&CE, and routes data into the Reconfigurable Pixel Processor (RPP) card. The RPP performs image flip and real-time NUC using up to 16 breakpoints, with a variety of other DSP functions such as image rotation, overdrive/underdrive, convolution, and buss bar robbing compensation under development at SBIR. The C&CE architecture is scalable, and RPP cards may be cascaded to increase DSP capability as real-time functions are developed in the future. Both TIP and RPP designs have been developed by Eglin AFB/KHILS under the PC-Based Array Control Electronics (PACE) program.

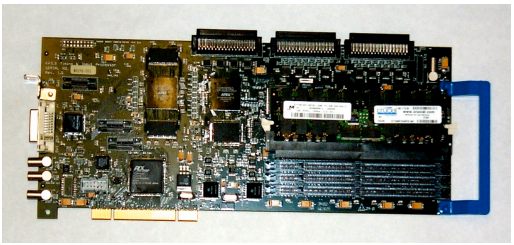

Figure 6a – Next-Gen Input Card

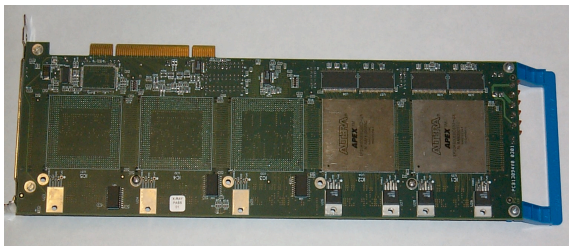

Figure 6b – Next-Gen Pixel Processor Card

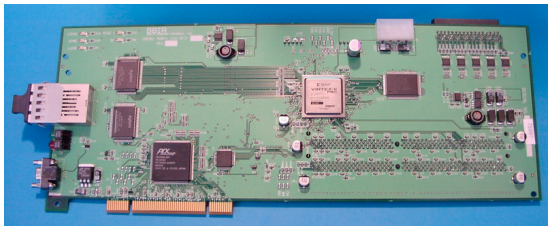

Figure 6c – Next-Gen Output Card

Design validation is complete for the TIP, RPP, and MIRAGE 1/1.5 output boards. The cards have been integrated into a single PCI chassis, and have collectively been demonstrated driving a MIRAGE 1 DEE. System software, GUI, and DSP firmware development is ongoing in support of MIRAGE 1.5, MIRAGE II, and LFRA projects.

6. CALIBRATION RADIOMETRY SYSTEM (CRS) & NUC DEVELOPMENT

The first-generation MIRAGE system included an optional CRS comprised of a 320 x 256 Indigo Merlin lab camera, an IR microscope lens, two blackbodies, a mechanical translation stage, an optical table, and control/NUC processing software, which ran on the system host computer[2]. In order to maximize NUC capabilities for the next-gen MIRAGE IRSP systems, an upgraded CRS is in development.

The new CRS will use the same type of camera, but will have a three-step variable magnification IR NUC lens optimized for performing full-array, sparse grid NUC on MIRAGE 1, MIRAGE II, and legacy IRSP arrays. The CRS will still use multiple thermal references during the calibration and NUC collection process, but will offer an improved layout for the most efficient reference and emitter array map collection. The first NUC collection algorithm developed for the new CRS will mirror that presented previously by Hust and Lippert[1], with the future goal to incorporate the latest techniques published by Williams, *et al*.

The following outlines the basic NUC collection and data processing algorithm.

1. CAMERA NUC – Characterize over temperature and integration time,

2. OPTICAL ALIGNMENT – Camera to DEE,

3. BLURRING – Minimize effects of (potential) non-unity fill factor,

4. CHARACTERISTIC CURVE – Characterize radiance vs. drive for typical pixels,
   a. RAW ARRAY MAP – Identify bad pixels,
   b. 2-D AVERAGING AT LOW-TEMP – Improve SNR at low end of range (TBD),
   c. VARY INTEGRATION TIME/ATTENUATION – For high-temp range,

5. INVERSE CHARACTERISTIC CURVE – Linearize radiance as a function of input drive,

6. ACQUIRE ARRAY MAPS – Sparse stepped grid on emitter array with frame averaging,
   a. GRID POINTS 1-N - Collect all grid points at each drive level, then increase drive,
   b. 2-D AVERAGING AT LOW-TEMP – Improve SNR at low-temp range (TBD),
   c. VARY INTEGRATION TIME/ATTENUATION – For high-temp range,
   d. DEAD CAMERA PIXEL REPLACEMENT – Based upon raw array map,

7. NUC TABLE CREATION – Generation and upload of NUC breakpoint LUT(s) into C&CE

8. COMPUTATION – Generate gain and offset entries for multi-point NUC table,

9. UPLOAD NUC LUT – Transfer NUC coefficients into C&CE memory,

10. CHECK ARRAY NON-UNIFORMITY – Quantify errors at and between break points.

Figure 7 – First-stage NUC Algorithm for Next-generation CRS

Algorithm details are currently being defined, in order to optimize collection time/camera NUC, and resolve use of variable integration time vs. ND filtering at the high end of the emitter dynamic range.

7. SUMMARY

SBIR is expanding the original MIRAGE turnkey IRSP technology into an advanced next-generation capability for a variety of scene projection applications. With the MCNC-RDI emitter foundry online, prototype arrays packaged and ready for test, LFRA wafers being probed, the MIRAGE II RIIC ready for fabrication, and critical next-gen C&CE technologies successfully demonstrated, SBIR is moving forward successfully on multiple technical fronts. These product developments will expand current IRSP capabilities and provide core simulation technology for emerging sensors.

ACKNOWLEDGMENTS

The authors would like to thank Eglin AFB/KHILS for their PACE electronics development efforts, the Tri-Services IRSP Working Group for their support of LFRA, and Dr. Owen Williams for his continuing research and advancement of IR scene projection physics.

REFERENCES

1. David Hust, Jack Lippert, "Automated NUC Procedure for a 512 x 512 IR Array Using a 256 x 256 Camera, *Technologies for Synthetic Environments: Hardware-in-the-Loop Testing VI*, Proceedings SPIE Vol. 4366, (2001).

2. A. Irwin, J. Oleson, and Richard Robinson, "MIRAGE: Calibration and Radiometry System", *Technologies for Synthetic Environments: Hardware-in-the-Loop Testing V*, Proceedings SPIE Vol. 4027, (2000).