MIRAGE read-in-integrated-circuit testing results

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ABSTRACT

This paper describes the test results for the MIRAGE read-in-integrated-circuit (RIIC) designed by Indigo Systems Corporation. This RIIC, when mated with suspended membrane, micro-machined resistive elements, forms a highly advanced emitter array. This emitter array is used by Indigo and Santa Barbara Infrared Incorporated in a jointly developed product for infrared scene generation, called MIRAGE. The MIRAGE RIIC is a 512 x 512 pixel design which incorporates a number of features that extend the state of the art for emitter array RIIC devices. These innovations include an all-digital interface for scene data, snapshot image updates (all pixels show the new frame simultaneously), frame rates up to 200 Hz, operating modes that control the device output, power consumption, and diagnostic configuration. Tests measuring operating speed, RIIC functionality and D/A converter performance were completed. At 2.1 x 2.3 cm, this die is also the largest non-stitched device ever made by Indigo's foundry, American Microsystems Incorporated. As with any IC design, die yield is a critical factor that typically scales with the size and complexity. Die yield, and a statistical breakdown of the failures observed will be discussed.

Keywords: Infrared, Scene generation, Scene simulation, Hard-Ware-In-the-Loop, HWIL, MIRAGE, Emitter, Microstructure, RIIC

1. INTRODUCTION

The value of infrared (IR) scene simulation in the development and ongoing testing of IR systems is widely recognized by both government and industry. Reduction in the cost of missile systems is realized through hardware in the loop testing that allows the full signal path to be dynamically exercised in a laboratory setting, reducing the need for costly missile test firings. The ability to perform accurate simulations in a lab setting also offers the promise of shorter development cycles for IR based imaging systems by giving developers more immediate access to data. As IR focal plane technology advances, there is a need for corresponding advances in the capability of scene simulation hardware. With increasing focal plane array sizes and frame rates, the data rate required for scene simulation increases. FPA features such as snapshot integration, where all the pixels in the FPA integrate at the same time, have become standard and place additional requirements on scene simulation hardware.

Last year, Indigo Systems Corporation and Santa Barbara Infrared Inc. along with Rockwell Science Center announced the joint development of MIRAGE (Multi-spectral Infrared Animation Generation Equipment), a new scene simulation system[1]. MIRAGE applies Rockwell's proprietary process for microstructure fabrication to emitter elements and utilizes a newly designed RIIC with a number of important advances over prior RIIC designs. The MIRAGE RIIC, fabricated in the second quarter of 1998, is the first to incorporate an all-digital interface and snapshot frame updates. In addition, special attention was paid to reducing scene dependent non-uniformity, resulting in a unique approach to power handling. This paper begins with a description of the MIRAGE RIIC design in section two. Sections three and four describe the test set-up and wafer level characterization results from probe testing, including yield of operable die for the first lot of wafers.

2. MIRAGE RIIC DESIGN

2.1. Emitter overview

The MIRAGE RIIC is designed to be mechanically mated to a 512 x 512 array of suspended membrane, resistively heated micro-emitters. Each micro-emitter element is electrically connected to one of the 512 x 512 RIIC unit cells, allowing individual control of the current driven through each emitter element during scene generation. The electrical connection to the emitter from the RIIC also serves as the mechanical support for the emitter structure and provides the thermal path for heat flow during operation. Figure 1 is a schematic representation of a single emitter showing the resistive portion of the emitter (1) suspended above the RIIC substrate (2) by the electrical connection (3).
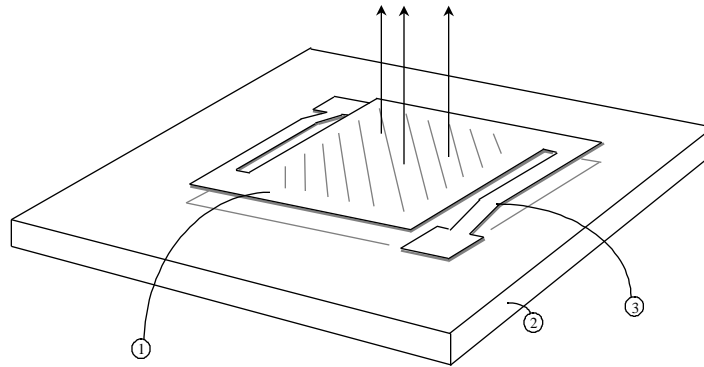
Figure 1. A schematic representation of a single emitter

2.2. RIIC signal chain

To generate a scene, the RIIC must be supplied with required bias voltages, timing, and formatted digital scene data. Figure 2 places the various RIIC functional blocks in the signal chain. The signal path starts with digital data input to one of the two 16 bit DAC's. These two DAC's work in parallel to generate analog voltages corresponding to emitter pixel radiance values. Each DAC generates voltages for a 512 row by 256 column area. The output voltage from each DAC is routed to one of 1024 column buffers where the voltage is sample and held and then driven up the column bus. The column buffers are organized in pairs by column. One buffer in the pair drives signals to odd rows, while the other buffer drives signals to the even rows.
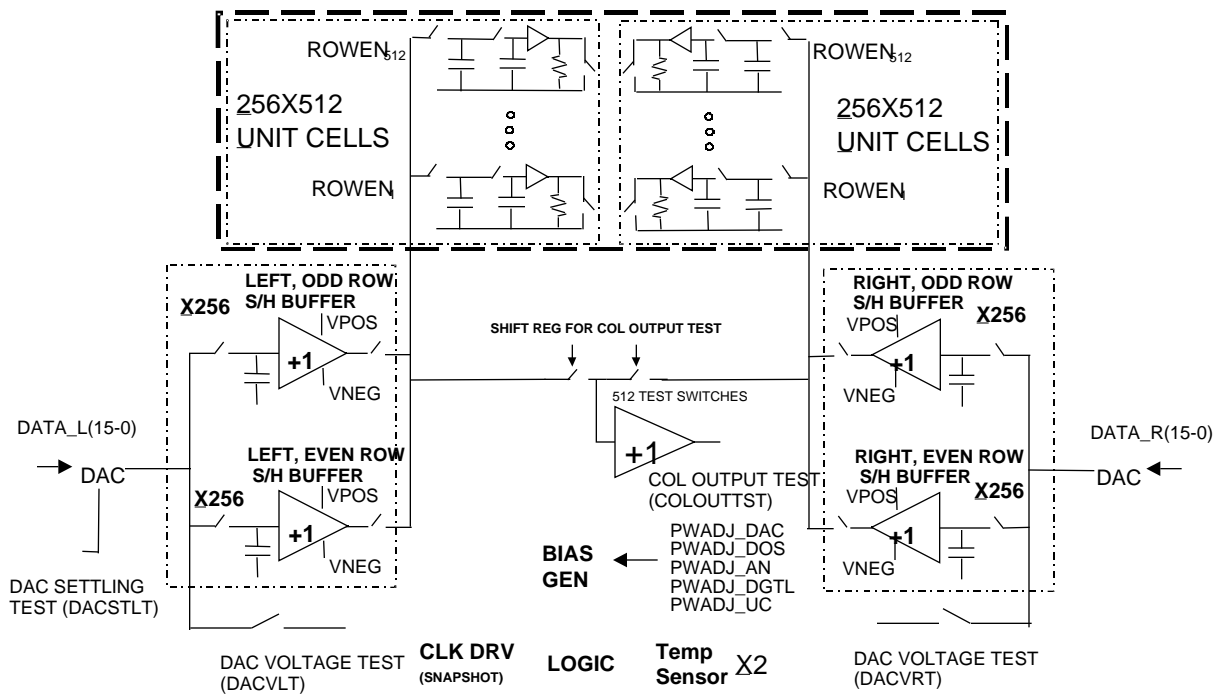

Figure 2. RIIC signal chain diagram

As the scene data for one row is received, converted, and routed to the appropriate column buffers (odd or even) the other set of buffers are writing the previous row of data up the column buses to individual unit cells. In this way, each buffer has an entire line time to allow the signal to settle, while the other set of buffers is being filled by the two DAC's. Right before each column buffer begins to drive its signal up the column bus, the row-enable switch in the appropriate unit cell along that column closes, allowing the signal to be received by that unit cell's sample and hold capacitor. Right before each column buffer is switched off, the row-enable switch closes, storing a voltage on the sample and hold capacitor. At the end of a

frame, when all 512 x 512 sample and hold capacitors are charged, the snapshot switches are simultaneously closed in every unit cell. Charge is shared between the sample and hold capacitor and the snapshot capacitor, creating a new drive voltage on each emitter driver and resulting in a new emitter radiant output.

In addition to the RIIC functional blocks that comprise the signal chain, there are a number of test circuits and different RIIC operating modes that may be accessed through six mode control bits. During normal operation these mode control bits allow the RIIC to operate in snapshot mode or alternately in rolling display mode by holding the snapshot switch closed all the time. The mode bits also allow the RIIC to operate in one of two current dissipation conditions. In the default operating condition, the total current through each unit cell is held constant, with more or less current shunted away from the emitter, depending on the voltage on the snapshot capacitor. The other current handling condition, current on demand, supplies to each unit cell only the current required to heat the emitter. Other mode bits allow the RIIC to be put into test configurations, where different parts of the signal chain may analyzed. Figure 2 shows lines that may be activated for DAC settling time testing or DAC output voltage testing. Figure 2 also shows a test shift register with a buffered output. The test shift register may be used to test the drive capability of each column buffer and to verify the current draw through any particular unit cell.

3. TEST SET-UP AND CONDITIONS

3.1. General Description

All initial MIRAGE RIIC characterization testing was performed at the wafer level. A probe card was used to make electrical contact with the RIIC bonding pads. This approach to characterization allowed much of the work done on initial design verification to be easily incorporated into the wafer probe screen testing of RIIC's for emitter array production. Testing was performed in a portable clean room at room temperature. Data was acquired by measuring the output from the various RIIC test points and by measuring the RIIC inputs during operation to find current draw or determine if proper operating voltages were maintained. Measurements were stored in either electronic format or in a laboratory notebook.

3.2. Test Equipment

Table 1 lists the equipment used during characterization testing.

Item	Part # / Serial #
Test Station #2	N/A
Electroglas Prober (8 in.)	2001X
VXI Interface Card– Indigo Custom	250-0003-09 Rev 1.0 / 0004
HP Switcher	3488A / 245389212
Probe Card – Indigo Custom	250-0002-09 Rev 1.0 / 0002
Fluke DMM	77 / Any in lab
Tektronix Oscilloscope	TDS 754C /
HP Parameter Analyzer	4145A / 2515J02393
Probe Card Jumper List & Supplements	N/A

Table 1. RIIC characterization test equipment

3.2.1. Test Station Description

The test station used for characterization testing is one of three identical test stations designed to allow flexible characterization and production testing of mixed signal integrated circuits. The primary components of the test station are programmable power supplies, a timing generator, a switch matrix, a precision volt/current meter, and an analog to digital converter. These test station components are all connected and controlled by a VXI backplane, allowing computer interface control.

4. CHARACTERIZATION TEST RESULTS

Characterization testing for the MIRAGE RIIC can be divided into three general areas of investigation: verification of functionality, signal chain measurements, and miscellaneous testing. Verification of functionality consists of measurement of current draw on the various bias supplies, and the verification of proper response to input timing and proper operation of RIIC logic for selecting the various operating modes. The signal chain measurements consist of DAC output voltage measurements, DAC settling time, column buffer output measurements, and unit cell current measurements. Other measurements include characterization of the on-chip temperature sensors and measurement of the electrical resistance of the current return path through the RIIC substrate.

4.1. RIIC timing and logic

The timing and logic are verified by direct and indirect means. The row and column shift registers have test outputs that can be monitored. Timing that is sent to the RIIC clock input pads will result in signals that come out on the test inputs. This verifies that timing is reaching the shift registers properly. Additionally, changes in the timing will affect the operation of the RIIC. When these changes are made and the RIIC performs as expected, the logic is verified. The types of changes made include changing the number of "dead" clocks at the end of a line of timing, performing a frame reset before a full frame has been clocked out, and increasing or decreasing the pixel clock frequency.

For all of these tests, the RIIC operated exactly as expected. During the course of this aspect of characterization, the logic was verified over frame rates from 1 Hz to over 200 Hz. The operating modes of the RIIC were also verified. This verification was an integral part of the overall characterization, since many of the possible operating modes allow the RIIC to operate in a specific test output mode. Table 2 summarizes the results of these verification tests.

Function	Pass / Fail
Frame reset	Pass
Row shift register	Pass
Column shift register	Pass
Pixel clock	Pass
Mode bits 0-5	Pass
Test shift register	Pass

Table 2. Summary of test results for timing and logic verification

4.2. Current draw measurements

Current draw is a critical test of general RIIC functionality. Insufficient current on a particular bias line can indicate a design problem or the potential for decreased output levels in an otherwise functional design. Greatly increased power draw on a specific bias voltage can indicate an IC processing defect that results in a short circuit between power supply lines and their returns. Power draw on the VDACPOS, VPOS, and VPD bias lines were measured and fell within the expected range based on initial simulations. While the primary purpose of characterization testing is IC design validation, some data was also obtained on failure rates. Measurements on the first wafer (44 die) show no current draw failures, indicating that the fabrication process at the foundry has very low defect levels.

Bias Voltage Name	Simulation Current	Measured	Pass / Fail
VDACPOS	< 200 mA	140 mA ± 20 mA	Pass
VPOS & VPD	< 30 mA	20 mA ± 5 mA	Pass

Table 3. Comparison between measured current values and initial RIIC simulations

4.3. Temperature sensor characterization

The RIIC has two temperature sensors located on opposite sides of the IC. These temperature sensors will be used to maintain a stable emitter substrate operating temperature. This is a critical feature of the RIIC, since emitter fill factor of roughly 50%, allows the substrate temperature to contribute to the overall radiance of the generated scene. Both temperature sensors are functional and have output that can be used for temperature control. The plot of temperature versus output voltage shows that the output is linear as expected and has a gain of -6 mV/ °C. This gain is somewhat lower than the expected value of –8 mV/ °C obtained through simulation, but it is within tolerances associated with this part of the IC design. More importantly, the temperature sensor will serve its purpose as part of the MIRAGE emitter substrate temperature control circuit. Figure 1 shows a plot of the temperature sensor output as a function of the wafer temperature. The dotted line is a least squares fit to those data points. The line's equation shows a slope of -6.1 mV/ °C.
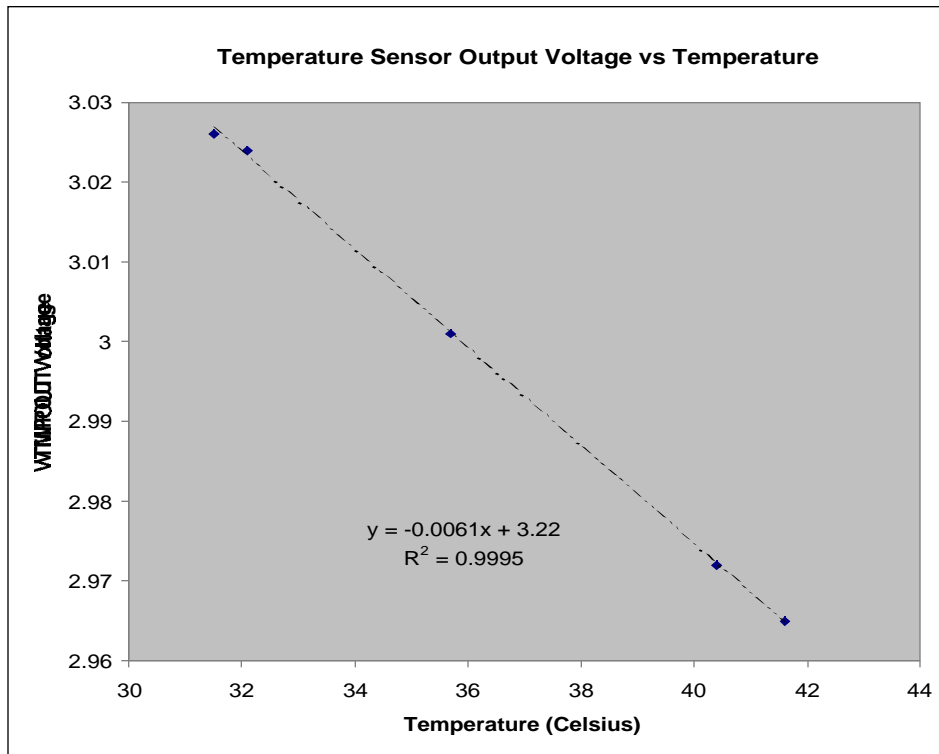

Figure 3. Graph of temperature sensor output voltage versus RIIC temperature

4.4. Resistance of current return path

The emitter current return path runs from the emitter return leg, down into the RIIC active circuitry, and out through the RIIC silicon substrate. The exact resistance is an important aspect of the design, since it determines how much of the voltage drop in the emitter drive current will occur in the emitter and how much will occur in the RIIC substrate. Initial modeling of the resistance indicated a value of roughly 1000 ohms per unit cell. Measurement of this value across 5 die on wafer # 1 resulted in an average value of 675 ohms. This value will allow even more of the emitter drive power than was initially modeled, to be dissipated in the emitter, resulting in slightly higher maximum temperatures.

4.5. DAC output voltage measurements

The RIIC has two 16 bit on-chip digital to analog converters (DAC's) that take as input a 16 bit word from the scene generation hardware and output a voltage that is used to drive individual emitters. Two test pads on the RIIC allow the output from each DAC to be characterized. Several aspects of the output were measured, including output voltage range, DAC bit steps, and a qualitative assessment of linearity

4.5.1. Output Voltage Range and Linearity

The output voltage range was predicted to be 0.5 to 3.55 volts. This range is a nominal value since there is also on-chip adjustment for the DAC current (which affects the output range) and DAC offset level. The output range for every RIIC die measured was either within the nominal range with no adjustment required or could easily be adjusted to fit within the nominal range. Figure 4 below shows a DAC's output voltage response to an input voltage ramp. The total output range for this DAC is shown to be 0.61 to 3.57 volts and is typical of the output response to an input ramp. The linearity of the output can also be seen in this plot. A coarse examination of the output plot shows a slight deviation from a straight line at the upper end of the range. This output corresponds to the expected output generated by the simulation.

One deviation from the simulation that was noted and investigated was an offset of 0.2 – 0.3 volts between the right and left DAC outputs. With normal grounding via the two VSUB pads, the right DAC output's zero level (all bits zero) was lower than the left DAC. The total dynamic range was typically 0.1 volts greater for the right DAC. Experiments in which one or the other VSUB grounds was removed yielded inconclusive results except that grounding seems to be at the heart of this anomaly. It is thought that the VSUB ground used during operation will eliminate this offset effect. If the effect remains, it will result in roughly a 10% reduction in system dynamic range.
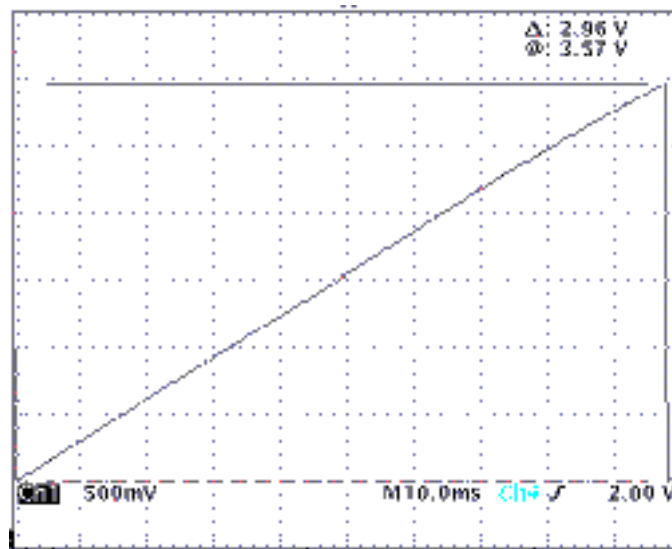

Figure 4. DAC output response to input data ramp

4.5.2. DAC Bit Measurements

In addition to the ramp, each bit of the DAC was enabled singly (that bit on and all the others off) and that level was programmed into the DAC for an entire row of output. This was done to determine that all the bits were present, to compare the bit step sizes, and to verify that the upper 8 bits and the lower 8 bits overlapped in output level. The overlapping of the upper and lower bits was an intentional aspect of the design. Figure 5 shows the stair step output of the upper bits toggled singly. Also visible in figure 5 is the beginning of the voltage ramp. The lower 8 bits are in the output but can not be resolved in this plot. Figure 6 shows the overlap in output range between the lower 8 bits and the upper 8 bits. Figure 7 shows the lowest 6 bits in the DAC output range. The LSB level in this test is only settled for a short time. Figure 8 resolves the LSB level better by programming that level into the middle of the output of bit nine.

4.6. DAC settling time

DAC settling time is an important aspect of the RIIC performance since the settling time places an upper limit on the fastest frame rate that can be displayed by the MIRAGE system. Based on a design goal of 200 Hz, the rise time and fall times for the DAC need to be less than 37 nanoseconds. The measured values for the rise and fall times were 19 and 18 nanoseconds respectively. Figures 9 and 10 show the DAC rise and fall time for a transition between the maximum output level and the minimum output level. While there is considerable noise on the signal, the transition is clearly visible for both measurements.
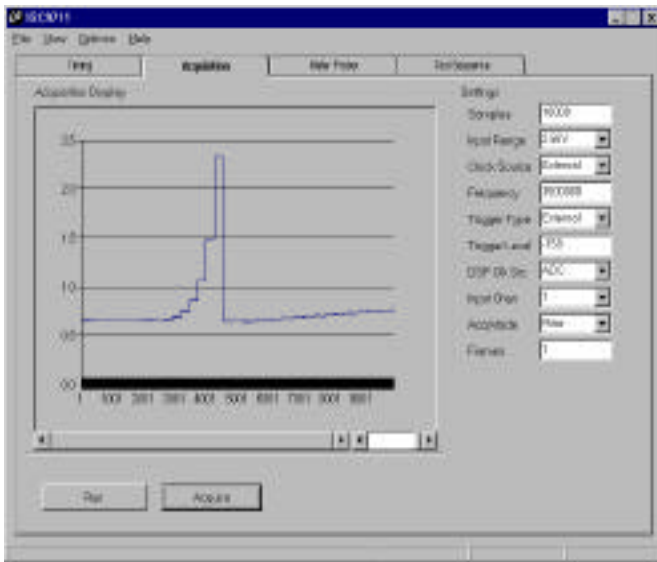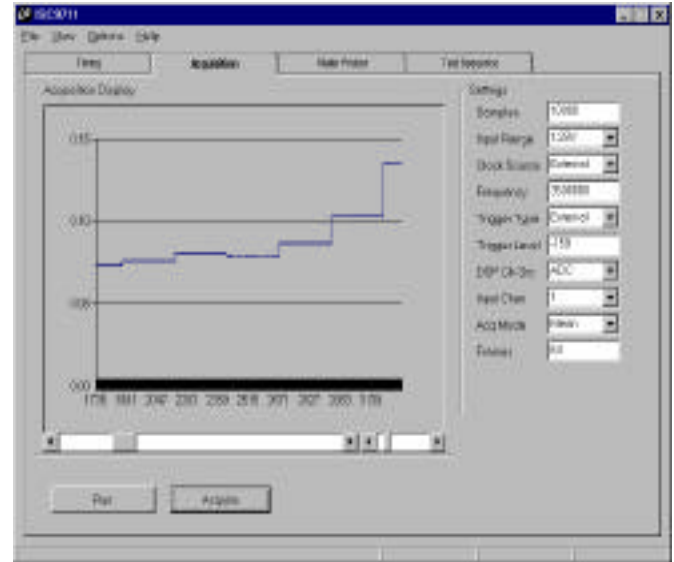
Figure 5. Each bit toggled singly

Figure 6. Overlap between upper and lower 8 bits
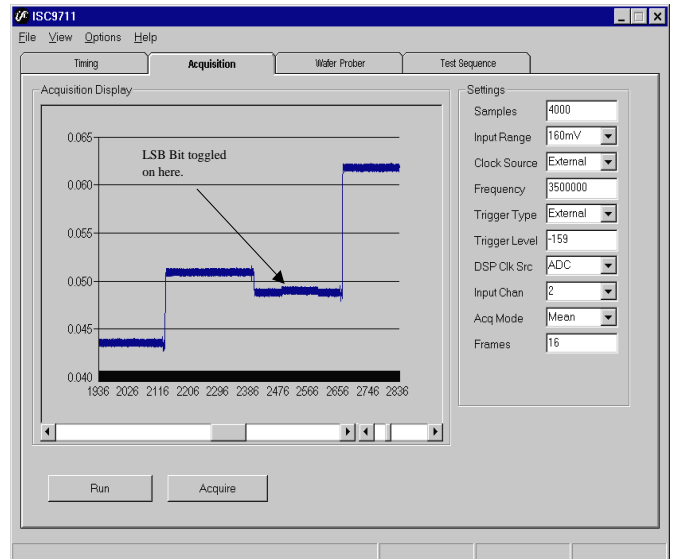

Figure 7. Lowest six bits resolved

LSB Bit toggled on here.

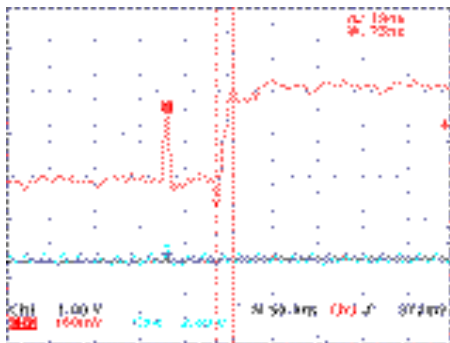Figure 8. LSB bit enabled on top of bit 9
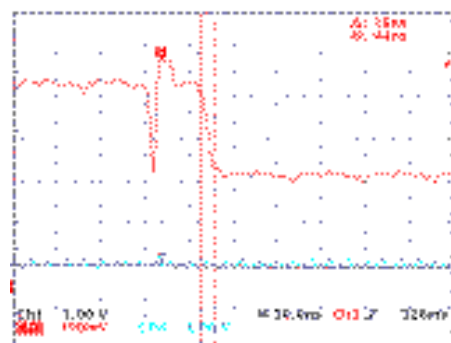

Figure 9. DAC rise time

Figure 10. DAC fall time

4.7. Column buffer output measurements

The buffers that drive the DAC voltage signal up the column bus lines can be tested by using the COLOUTTST test pad on the RIIC. By placing the RIIC into the column test mode and monitoring the output of this test pad, the next step in the signal path can be characterized. The output range of these buffers was measured by sending a DAC signal of maximum to every buffer and then the minimum value to each buffer. The offset between the left and right DAC outputs was again noticed in this test. The signal difference was compared to the simulation and was within the range of values expected for that part of the circuit. This test will also be used to screen die for column buffer defects during production testing. Figure 11 shows the output for the full column test that exercises all 1024 of the buffer amplifiers. Figure 12 shows the output for the first several column buffers. The sixth buffer shows a reduced output level of roughly 0.25 volts, indicating a problem with that channel. This type of defect was only observed on one die during initial characterization testing
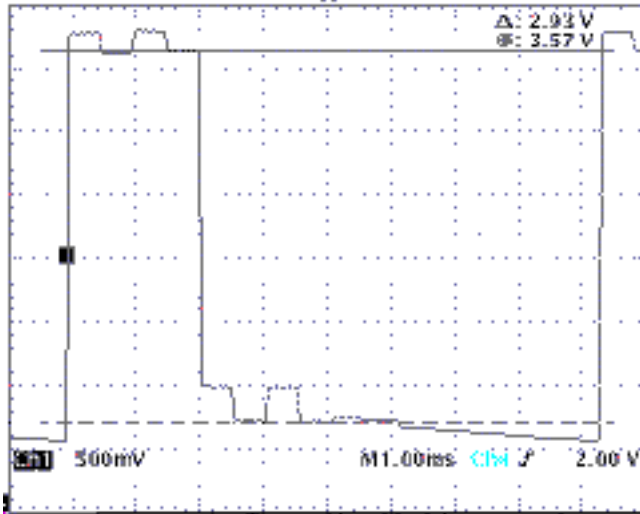

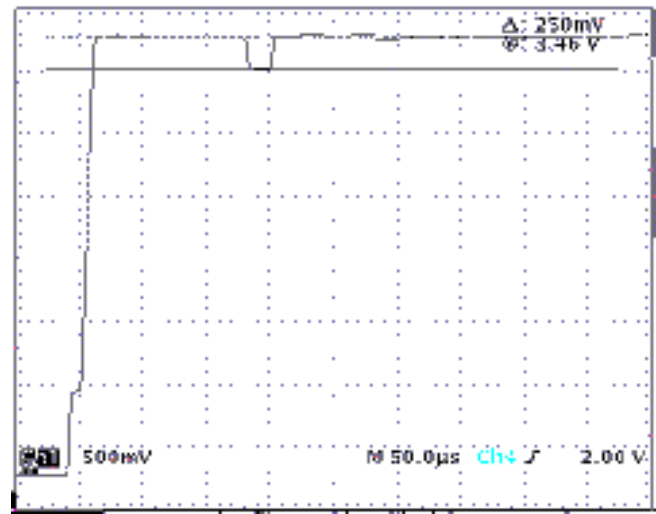Figure 11. Column buffers show expected dynamic range

Figure 12. Sixth column, odd row, buffer shows output variation.

4.8. Unit cell current measurements

The RIIC unit cell test mode allows current to be passed through a test transistor (instead of an emitter). This test allows a measurement of the full scale current draw in the unit cell. This is an important measurement, since the current through the unit cell must not limit the voltage that can be applied to the emitter. The nominal value for this current draw is roughly 100 micro-amps of current. During production testing, this current test can be applied to every unit cell to verify proper function and ensure high emitter operability. For characterization testing, this value was measured for individual pixels to validate the design. The measured value for the current was 96 microamps. This value is close to the 100 microamps and sufficiently validates the design. Additionally, the exact current in the unit cell can be changed through a unit cell current adjustment pad on the RIIC. Figure 13 shows the current demand full scale range of roughly 96 mV. In this measurement, one millivolt corresponds to one microamp of current.

4.9. Constant current verification

In most operating scenarios, the RIIC will be operated in constant current mode as described in section 2.2. However, under probe test conditions, testing the constant power mode is not practical due to limitations in heat sinking and in supplying the required current. The verification of constant current was made by integrating an RIIC die onto a specially designed fanout board, allowing the necessary heat sinking and supplying a low impedance path for the required current. As simulated, the RIIC draws 30 amps of current when operated in constant current mode.
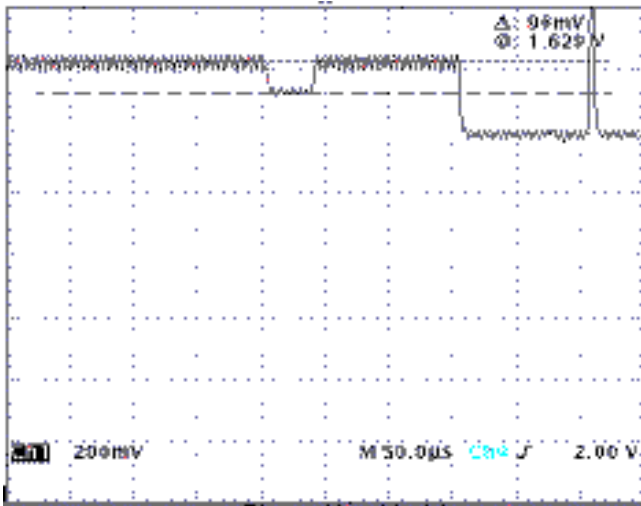
Figure 13. Current draw (96 millivolts = 96 microamps)

4.10. Operability of engineering lot

The MIRAGE RIIC design was fabricated on 8-inch wafers at containing 44 die per wafer. An initial engineering lot of five wafers was made in the first production run. Each die was tested for proper current draw, DAC operability, and column buffer full scale range. The yield for these first wafers was 87%, resulting in 192 usable die out of 220 possible. The most common defect was a failure of one or more column buffers to pass the full scale swing requirement.

5.   CONCLUSION

The MIRAGE RIIC is very different from previous RIIC designs because of its all digital interface and unique constant current operating capacity. Characterization of the design provided the needed confidence to begin work on emitter array fabrication. This work is proceeding. The data gathered during characterization testing on DAC settling time provides assurance that system level design decisions to operate up to 200 Hz are in line with expected performance. Data gathered on the temperature sensor output has been valuable as a verification tool for interim system level integration. Subsequent data on operability provides confidence that the present design is producible and could easily be scaled to larger devices without jeopardizing RIIC yield.

REFERENCES

1.   R. Lane, J. Heath, *Innovations in IR Scene Simulator Design,* SPIE Vol. 3368, p. 78-87, Orlando, Florida, 1998.