# Development of an Ultra-High Temperature Infrared Scene Projector at Santa Barbara Infrared Inc.

Greg Franks<sup>a</sup>, Joe LaVeigne<sup>a</sup>, Tom Danielson<sup>a</sup>, Steve McHugh<sup>a</sup>, John Lannon<sup>b</sup>, Scott Goodwin<sup>b</sup>

<sup>a</sup>Santa Barbara Infrared, 30 S Calle Cesar Chavez, Suite C, Santa Barbara, CA 93103 <sup>b</sup>RTI International, 3021 Cornwallis Rd., Research Triangle Park, NC 27709

## ABSTRACT

The rapid development of very-large format infrared detector arrays has challenged the IR scene projector community to develop correspondingly larger-format infrared emitter arrays to support the testing needs of systems incorporating these detectors. As with most integrated circuits, fabrication yields for the read-in integrated circuit (RIIC) that drives the emitter pixel array are expected to drop dramatically with increasing size, making monolithic RIICs larger than the current 1024x1024 format impractical and unaffordable. Additionally, many scene projector users require much higher simulated temperatures than current technology can generate to fully evaluate the performance of their systems and associated processing algorithms.

Under the Ultra High Temperature (UHT) development program, Santa Barbara Infrared Inc. (SBIR) is developing a new infrared scene projector architecture capable of producing both very large format (>1024x1024) resistive emitter arrays and improved emitter pixel technology capable of simulating very high apparent temperatures. During an earlier phase of the program, SBIR demonstrated materials with MWIR apparent temperatures in excess of 1000K. New emitter materials have subsequently been selected to produce pixels that achieve even higher apparent temperatures. Test results from pixels fabricated using the new material set will be presented and discussed. Also in development under the same UHT program is a 'scalable' RIIC that will be used to drive the high temperature pixels. This RIIC will utilize through-silicon vias (TSVs) and quilt packaging (QP) technologies to allow seamless tiling of multiple chips to fabricate very large arrays, and thus overcome the inherent yield limitations of very-large-scale integrated circuits. Current status of the RIIC development effort will also be presented.

Keywords: UHT, Infrared Scene Projection, Through-silicon Via, Quilt Packaging, Hardware-in-the-loop

## 1. INTRODUCTION

Santa Barbara Infrared (SBIR) is a world leader in the development and production of infrared scene projector systems (IRSPs) that meet the needs of hardware-in-the-loop (HWIL) simulation testing. SBIR's multi-spectral infrared animation generation equipment (MIRAGE) offers the most advanced performance available in resistive array-based IRSPs. As sensor and seeker technology evolves, new performance demands will be placed on the IRSP systems used to test them. SBIR is responding to these demands with the development of the next generation of resistive array scene projector technology. The UHT program is funded by the Test Resource Management Center (TRMC) Test and Evaluation/Science & Technology (T&E/S&T) Program through the U.S. Army Program Executive Office for Simulation, Training and Instrumentations (PEO STRI). The program's goal is the design, assembly, and test of an updated IRSP system that will offer performance increases in apparent temperature, speed and spatial resolution.<sup>[1]</sup>

Infrared Imaging Systems: Design, Analysis, Modeling, and Testing XXVI, edited by Gerald C. Holst, Keith A. Krapels, Proc. of SPIE Vol. 9452, 94520W · © 2015 SPIE · CCC code: 0277-786X/15/\$18 · doi: 10.1117/12.2177448

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In order to achieve improvements in each of these metrics, development efforts in the area of each subcomponent are being pursued. New emitter pixels that leverage the basic design foundation of existing MIRAGE pixels, but incorporate new materials and geometries have already demonstrated promising performance in early tests. The latest pixels are expected to reach the program goal of 1500 K MWIR apparent temperature in the next round of testing. In addition, the design of a new read-in integrated circuit (RIIC) that will support a faster frame rate requirement of 500 Hz and the increased power required by higher temperature pixels has recently been completed and is ready for fabrication. The design of this RIIC will also support array quilt packaging, the process by which multiple discreet RIIC tiles are packaged together to produce one composite large emitter array. Finally, the performance of this new RIIC will drive the design new drive electronics with the capability to accept simulation scene data and send it into the RIIC at the necessary high frame rates and low noise levels.

#### 2. BACKGROUND AND GOALS

The UHT program calls for advancement in essentially every performance metric of the resistive array-based IRSP. This includes a MWIR apparent temperature increase from 700 K to over 1500 K (see Figure 1), a frame rate increase from 200 Hz to 500 Hz, and support for array formats of up to 2048 x 2048 pixels. The first phase of the UHT program was completed approximately one year ago. During this phase, the first emitter pixels incorporating new materials and geometries were fabricated and tested.<sup>[2]</sup> These pixels produced significantly more radiance than legacy pixels, and the data collected drove additional design modifications for the second program phase.

SBIR also conducted a large array trade study during the first phase of the UHT program.<sup>[3]</sup> This study determined the optimum design approach for creating a RIIC that would support both high frame rates and high spatial resolution. It identified quilt packaging as the optimum method for producing very large arrays that could run at high frame rates. This quilting approach was made feasible due to the advancement of two key technologies and fabrication processes. The first is the fabrication of the quilt packaging nodules that enable alignment of neighboring RIIC tiles with minimal gap between tiles. The second is the fabrication of through-silicon-vias that allow for the RIIC signals to be routed through the back side of the chip instead of through bond pads on the edges. These steps led to the launch of a new RIIC design at the beginning of the second phase of the program.



Figure 1 Pixel performance evolution across program phases as a function of radiance and apparent temperature

# 3. UHT EMITTER PIXEL DEVELOPMENT

Early in the second phase of the program, additional modifications to the material used for the dielectric and leg layers of the emitter pixel were tested. Figure 2 highlights the important pixel structural components for reference. Prior to their use in fully-formed pixel structures, the new materials were tested in the form of bulk film stacks at very high temperatures. These stacks were annealed at temperatures above 1500 K, and then analyzed to confirm material survivability and the absence of undesired layer interactions at high temperatures. This successful test was a relatively fast and inexpensive indicator that the new materials would perform at temperature in fully formed pixel structures.



Figure 2 Conceptual drawing of pixel structure showing key components that are responsible for electrical (leg and resistor), mechanical (plug and bridge) and optical (absorber and reflector) performance.

Pixel structures were subsequently fabricated using numerous different geometries with multiple goals in mind. The first was to increase the fill factor so that the apparent temperature of the pixel (based on its in-band radiance output) would be much closer to its actual physical temperature. Improved photolithography processing successfully increased the fill factor from about 60% to approximately 80%. The second goal of the updated pixel geometries was to improve mechanical performance at high temperatures. Finite element analysis (FEA) was used to determine those geometries that would best respond to thermally-induced stress and would exhibit minimum warping at very high temperatures.

During the test pixel fabrication period, another method for collecting electrical and radiometric data not available in bulk film testing was explored. A new "fast-turn" pixel structure was created by depositing films directly onto the silicon substrate, as opposed to depositing onto a polyimide spacer layer in a standard pixel. These direct-on-silicon stacks were transformed into suspended bridge structures by etching away the silicon substrate underneath them. While the resulting pixel lacks the tuned optical cavity and reflector of a standard pixel, and produces less radiance for a given physical temperature, it can be produced faster and at lower cost than a standard pixel. This makes it a very valuable tool for gathering data on prospective pixel design modifications prior to committing to expensive and lengthy standard fabrication runs.

Both the fast-turn and the fully-formed test pixels were electrically and radiometrically characterized at SBIR upon completing fabrication and packaging. The fast-turn pixel was successfully driven to a maximum MWIR apparent temperature of just over 1000 K, requiring just over 2 milliwatts of input power to achieve this temperature. Adjusting for the lower emissivity and fill factor of this version of the pixel shows that it reached a similar physical temperature as that which would produce approximately 1500 K in a standard pixel. This confirmed the viability of the new materials in terms of high temperature survivability and power consumption. As expected, the standard pixel produced even higher apparent temperatures. Multiple geometries achieved greater than 1400 K MWIR apparent temperature (see Figure 3). The hottest structure tested reached 1490 K, or nearly 20 times the radiance produced by legacy pixels currently used in IRSP systems. It did so while drawing only 2.3 mW of power, and displayed a well-behaved temperature coefficient of resistance curve (see Figure 4). While this level of power consumption is roughly four times that of legacy pixels, it is much less than initial estimates of the power required to reach this temperature, and is compatible with the latest RIIC emitter unit cell designs.



Figure 3 Pixel geometries that achieved the highest MWIR apparent temperatures

Rise and fall time of the test pixels were also measured. The rise time was approximately 2.1-2.2 milliseconds, which approaches the speed necessary for full transitions at 500 frames per second. The fall time was approximately 3.5 milliseconds, but thus far, has only been measured for a single pixel geometry with a very long leg. The long leg has the effect of increasing fall time by slowing conduction of heat out of the pixel as it approaches its temperature floor. Modeling results indicate that a pixel with standard leg lengths will achieve fall times under 2 milliseconds.

A pixel fabrication run to produce and test the finalized emitter design has been initiated and will be completed in the summer of 2015. These test pixels are expected to have 2 millisecond or better rise and fall times to support the 500 Hz frame rate goal. They are also expected to consistently perform at or above the program goal apparent temperature of 1500 K when test pixels are characterized, and will be the design that is combined with the new RIICs upon their fabrication to produce an operable ultra-high temperature emitter array.



Figure 4 Power vs radiance curve for the hottest pixel tested to date. Each red data point represents an incremental step up in drive current

# 4. UHT RIIC DEVELOPMENT

After the large array trade study confirmed quilt packaging as the optimal path to larger and faster emitter array formats, a new read-in integrated circuit (RIIC) design was initiated. The design requirements dictated by desired system performance of the next generation of IRSPs necessitated upgrades over existing RIICs in all key performance metrics. First, this design had to support operation at 500 frames per second. Next, the RIIC emitter unit cell driver circuit would have to provide significantly more power, on the order of a few milliwatts. Finally, the design would have to be scalable, meaning that it would need to support quilt packaging along at least three of its four edges to permit the fabrication of larger arrays from multiple RIIC tiles.

The current design accommodates QP nodules on three of its four sides as shown in Figure 5. The fourth side uses conventional bond pads for signal input/output via bond pads, while emitter power and ground are routed through the backside via TSVs (see Figure 5). An additional goal for this layout was its use of repeatable modular stitch blocks to build up the entire 512-column-by-768-row full-size tile. This approach was expected to reduce the cost and time necessary to execute any future design transition to alternate tile sizes and/or the potential use of TSVs for all signal routing to enable quilting on all four sides.



Figure 5 SEM images of assembled quilt package nodules (left) and TSVs (right)In order to achieve the increased clock and data rates necessary for 500 Hertz operation, the design balanced a trade space between number of inputs and signal propagation speed along a given trace. The design settled on using 32 parallel analog data input lines, a number that was found to be an ideal balance between available bandwidth per channel and simplicity of trace routing. These inputs will require off-chip digital-to-analog converter (DAC) electronics with high speed and low noise outputs in order to support the desired frame rates. Within the next year SBIR will be designing drive electronics that satisfy this need.

The previously discussed testing of new emitter designs provided important insight on the maximum power level the unit cell driver in the new RIIC would have to achieve. As a result, the unit cell design will be capable of providing 3.2 mW to the emitter pixel at maximum. This power level will drive the finalized emitter design above 1500 K MWIR apparent temperature, while leaving sufficient margin to account for small variations in resistance across different emitter pixels. In addition, the use of TSVs for both emitter power and ground not only facilitates quilting, but also offers another advantage. By evenly spacing the TSVs (and thus the available connections to emitter power and ground) at a density of two power TSVs and two ground TSVs per 32 x 32 block of pixels, the resulting IR drop across the chip in a maximum power scenario will be very small. Whereas non-uniformity due to IR drop during simulations on legacy designs was very noticeable when many pixels were driven very hot, corresponding simulations show that the new design has a maximum voltage drop of less than 1% of the input voltage range for similar conditions (see Figure 6). This improvement was achieved despite the pixels drawing roughly four times the current per unit cell.



Figure 6 Map of voltage drop across a simulated 64 x 32 section of the RIIC with all emitters running at maximum power. The largest drop, which occurs farthest away from the upper pair of power TSVs, is 30 mV or under 1% of the full drive range.

Due to its large size, the RIIC uses a stitched design. The stitch blocks have been designed to make the fabrication of other chip sizes relatively simple. Simplicity of design evolution is key to paving the way to large format, ultrahigh temperature scene projector systems based on quilted RIICs. The current RIIC design is an important risk reduction step towards that goal. By proving the feasibility of TSVs for power supplies in a fully-functional RIIC and supporting quilting on three of four sides (while using conventional bond pads for noise-sensitive input data), this RIIC represents a measured approach to implementing these cutting edge technologies. After successful quilt packaging and operation of multiple 512 x 768 tiles, the ultimate goal is to use the data gathered and apply lessons learned to evolve the RIIC design into a new format that will route <u>all</u> signals through TSVs, and thus allow for quilt packaging on all four sides. This RIIC will be the core building block of future large format UHT IRSP systems.

## 5. SUMMARY

Advancements in the performance of each critical subcomponent of the next-generation infrared scene projector (IRSP) have been made, and further development in all of these areas is ongoing. The most recently tested emitter pixels have produced the highest radiance measured from a resistive emitter to date. That radiance, which corresponds to a MWIR apparent temperature of close to 1500 K, is almost 20 times higher than that produced by legacy pixels. Final design modifications to be implemented and tested in the near future will push pixel performance over the 1500 K target threshold. Simultaneously, the new RIIC that will drive these pixels – the design of which has just been successfully completed – will be fabricated and tested. This 512 x 768 pixel format chip will make use of TSVs and quilt packaging to create the first multi-tile composite emitter arrays. A parallel effort to design the drive electronics that feed image data to the emitter array at the necessary high speeds will occur in the same time frame. Upon their completion, these efforts will provide all of the necessary building blocks to produce the first very-large-format, ultra-high temperature IRSP systems.

## 6. **REFERENCES**

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